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10/582,035	05/07/2007	Zheng Shen	GWS-009	1665

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GOODWIN PROCTER LLP
PATENT ADMINISTRATOR
EXCHANGE PLACE
BOSTON, MA 02109-2881

EXAMINER	
HUBER, ROBERT T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,035	SHEN ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16* is/are rejected.

7)☒ Claim(s) *11,12,15,16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/07/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The disclosure is objected to because of the following informalities: Page 5, paragraph [0028] reads "FIG. 9 depicts a second aspect…" but should read "FIG. 9 depicts a seventh aspect". Appropriate correction is required.

4. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an

improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

5. The abstract of the disclosure is objected to because it is not descriptive of the invention. Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claims 11, 12, 15, and 16 objected to because of the following informalities: The use of the term “substantially” is indefinite and ambiguous since it is a relative term of degree. Therefore it is not given patentable weight. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 4, 13, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Perugupalli et al. (US 6,455,905 B1).

a. Regarding claim 1, Perugupalli discloses a monolithic structure (e.g. figure 8), comprising

a first lateral device having a first source terminal (top first source terminal), a first drain terminal (top first drain terminal), and a first gate terminal (tope first gate terminal), each of said first source, first drain, and first gate terminals terminating on a first surface of a semiconductor substrate (e.g. as seen in figure 8, with cross section in figure 7);

and a second lateral device having a second source terminal (bottom source terminal), a second drain terminal (bottom drain terminal) and a second gate terminal (bottom gate terminal), each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate (as seen in the figures 8 and 9, and disclosed in col. 5, lines 41 - 50),

wherein said first lateral device is combined with said second lateral device on said substrate (e.g. as seen in figures 8 and 9), said first source terminal is connected to said second source terminal to define a common source terminal of the monolithic structure, and a first electrically isolated lead comprises the common source terminal (source terminals are connect to each other via wire

bonding to the isolated lead 124, as seen in figure 8 and disclosed in col. 5, lines 14 – 19).

b. Regarding claim 3, Perugupalli discloses the monolithic structure of claim 1, as cited above, further comprising a second electrically isolated lead comprising said first drain terminal (figure 8, lead 144) and a third electrically isolated lead comprising said second drain terminal (figure 8, lead 143), wherein said first and second drain terminals are electrically independent of each other (e.g. as seen in figure 8).

c. Regarding claim 4, Perugupalli discloses the monolithic structure of claim 3, as cited above, further comprising a fourth electrically isolated lead comprising said first gate terminal (figure 8, lead 142) and a fifth electrically isolated lead comprising said second gate terminal (figure 8, lead 141), said first and second gate terminals being electrically independent of each other (e.g. as seen in figure 8).

d. Regarding claim 13, Perugupalli discloses a monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate (e.g. figure 8 and substrate disclosed in col. 2, lines 41 - 42), said structure comprising

a first lateral power transistor device comprising a first source terminal (top source terminal), a first drain terminal (top drain terminal), and a first gate terminal (top gate terminal), said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate (e.g. as seen in figure 8);

a second lateral power transistor device having a second source terminal (bottom source terminal), a second drain terminal (bottom drain terminal), and a second gate terminal (bottom gate terminal), said second source, second drain, and second gate terminals terminating on said first surface (e.g. as seen in figure 8), said first and second gate terminals being electrically independent of each other (e.g. as seen in figure 8); and said first and second drain terminal being electrically independent of each other (e.g. as seen in figure 8);

a first electrically isolated lead comprising said first source terminal connected to said second source terminal (top source terminal is connected to bottoms source terminal via wire bonds connected to lead 124, as seen in figure 8 and disclosed in col. 5, lines 14 - 19);

a second electrically isolated lead comprising said first drain terminal (lead 144);

a third electrically isolated lead comprising said second drain terminal (lead 143);

a fourth electrically isolated lead comprising said first gate terminal (lead 142); and

a fifth electrically isolated lead comprising said second gate terminal (lead 141).

e. Regarding claim 14, Perugupalli discloses the monolithic structure of claim 13, as cited above, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET (col. 3, lines 59 – 61, disclose the transistors to be LDMOS, which is defined to be laterally diffused MOSFET transistors in the Background, col. 1, lines 14 – 16).

9. Claims 1, 3 – 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Agata et al. (US 5,389,810).

a. Regarding claim 1, Agata discloses a monolithic structure (e.g. figures 11 - 14 and the Background of the Invention, col. 1, lines 30 - 65) comprising

a first lateral device having a first source terminal (source terminal extending from 1st transistor), a first drain terminal (terminal 120b), and a first gate terminal (terminal 140b), each of said first source, first drain, and first gate terminals terminating on a first surface of a semiconductor substrate (e.g. as seen in figures 13 and 14);

and a second lateral device having a second source terminal (source terminal extending from second transistor), a second drain terminal (terminal 120a) and a second gate terminal (terminal 140a), each of said second source,

second drain, and second gate terminals terminating on said first surface of the semiconductor substrate (e.g. as seen in figures 13 and 14),

wherein said first lateral device is combined with said second lateral device on said substrate (e.g. as seen in figure 14), said first source terminal is connected to said second source terminal to define a common source terminal of the monolithic structure (e.g. seen in figure 11 and 12), and a first electrically isolated lead comprises the common source terminal (lead 110 of figure 12, and also seen in figure 11 that source terminal are connect to a lead).

b. Regarding claim 3, Agata discloses the monolithic structure of claim 1, as cited above, further comprising a second electrically isolated lead comprising said first drain terminal (figure 13, lead 12a, and col. 1, lines 59 - 66) and a third electrically isolated lead comprising said second drain terminal (figure 13, lead 12b, and col. 1, lines 59 - 66), wherein said first and second drain terminals are electrically independent of each other (e.g. as seen in figures 11 and 13).

c. Regarding claim 4, Agata discloses the monolithic structure of claim 3, as cited above, further comprising a fourth electrically isolated lead comprising said first gate terminal (figure 13, lead 14a, and col. 1, lines 59 - 66) and a fifth electrically isolated lead comprising said second gate terminal (figure 13, lead 14b, and col. 1, lines 59 - 66), said first and second gate terminals being electrically independent of each other (e.g. as seen in figures 11 and 13).

d. Regarding claim 5, Agata discloses the monolithic structure of claim 3, as cited above, wherein said first gate terminal is connected to said second drain terminal and said second gate terminal is connected to said first drain terminal (e.g. as seen in figures 11 and 12).

e. Regarding claim 6, Agata discloses the monolithic structure of claim 1, as cited above, wherein each of said first and second lateral devices comprises a lateral power MOSFET (col. 1, lines 38 – 41 discloses the transistors to be MOSFETs, and figure 14 shows that they are lateral).

f. Regarding claim 7, Agata discloses a monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate (e.g. figures 11 -14 and the Background of the Invention, col. 1, lines 30 - 65), said monolithic structure comprising:

a first lateral power transistor device comprising a first source terminal (source terminal extending from 1st transistor), a first drain terminal (terminal 120b) and a first gate terminal (terminal 140b), each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate (e.g. as seen in figures 13 and 14);

a second lateral power transistor device comprising a second source terminal (source terminal extending from second transistor), a second drain

terminal (terminal 120a), and a second gate terminal (terminal 140a), each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate (e.g. as seen in figures 13 and 14), said first gate terminal being connected to said second drain terminal (e.g. as seen in figures 11 and 12), said second gate terminal being connected to said first drain terminal (e.g. as seen in figures 11 and 12), and said first and second drain terminals being electrically independent of each other (e.g. as seen in figures 11 and 12);

a first electrically isolated lead comprising said first source terminal connected to said second source terminal (lead 110 in figure 12, corresponding to lead 11 in figure 13);

a second electrically isolated lead comprising said first drain terminal (lead 120b of figure 12, corresponding to lead 12b of figure 13); and

a third electrically isolated lead comprising said second drain terminal (lead 120a of figure 12, corresponding to lead 12a of figure 13).

g. Regarding claim 8, Agata discloses a the monolithic structure of claim 7, as cited above, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET (col. 1, lines 38 – 41 discloses the transistors to be MOSFETs, and figure 14 shows that they are lateral).

10. Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Utsunomiya et al. (US 2002/0175373 A1).

a. Regarding claim 9, Utsunomiya discloses a monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate (e.g. as seen in figure 4), said structure comprising

a first lateral power transistor device (e.g. left side transistor) comprising a first source terminal (left source terminal 301), a first drain terminal (left drain terminal 302), and a first gate terminal (gate terminal 303), each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate (substrate 402 as disclosed in paragraph [0034]);

a second lateral power transistor device (e.g. right side transistor) comprising a second source terminal (right source terminal 301), a second drain terminal (right drain terminal 302), and a second gate terminal (gate terminal 303), each of said second source, second drain, and second gate terminals terminating on said first surface (e.g. as seen in figure 4), said first and second drain terminals being electrically independent of each other (e.g. as seen in figure 4);

a first electrically isolated lead comprising said first source terminal connected to said second source terminal (lead 103)

a second electrically isolated lead comprising said first drain terminal (lead 107);

a third electrically isolated lead comprising said second drain terminal (lead 108); and

a fourth electrically isolated lead comprising said first gate terminal connected to said second gate terminal (lead 106).

b. Regarding claim 10, Utsunomiya discloses the monolithic structure of claim 9, as cited above, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET (paragraph [0022] discloses the transistors are MOSFETs).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Utsunomiya in view of Green et al. (US 4,472,871).

a. Regarding claim 11, Utsunomiya discloses the monolithic structure of claim 9, but is silent with respect to the size of said second lateral power transistor being substantially smaller than a size of said first lateral power transistor. Green teaches that for multiple transistors on the same substrate, the

size of the second transistor may be smaller than the size of the first transistor (col. 4, lines 59 - 61).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Utsunomiya such that the second power transistor is smaller than the first, since Green discloses that it known in the art. One would be motivated to make such a modification since the electrical characteristics, such as the switching speed or current through the device can be affected by reducing dimension size.

b. Regarding claim 12, Utsunomiya discloses the monolithic structure of claim 9, but is silent with respect to a first threshold voltage of said first lateral power transistor being substantially different from a second threshold voltage of said second lateral power transistors and a difference in said first and second threshold voltages is at least ranging approximately 0.1 V. Green teaches that for multiple transistors on the same substrate the threshold voltages may be different by up to 1.75 V (e.g. table in col. 3).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Utsunomiya such that the threshold voltages of the two power transistors of a monolithic structure differ by over 0.1 V, since Green teaches that such modifications are known in the art. One would be motivated to make such a modification in order to allow for

more flexibility in circuit design, as well as for an increase in transistor switching speed, as disclosed in Green (col. 3, lines 52 - 53, and col. 4, lines 33 - 34).

13. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view of Green.

a. Regarding claim 15, Perugupalli discloses the monolithic structure of claim 13, but is silent with respect to the size of said second lateral power transistor being substantially smaller than a size of said first lateral power transistor. Green teaches that for multiple transistors on the same substrate, the size of the second transistor may be smaller than the size of the first transistor (col. 4, lines 59 - 61).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the second power transistor is smaller than the first, since Green discloses that it known in the art. One would be motivated to make such a modification since the electrical characteristics, such as the switching speed or current through the device can be affected by reducing dimension size.

b. Regarding claim 16, Perugupalli discloses the monolithic structure of claim 13, but is silent with respect to a first threshold voltage of said first lateral power transistor being substantially different from a second threshold voltage of said second lateral power transistors and a difference in said first and second threshold voltages is at least ranging approximately 0.1 V. Green teaches that for

multiple transistors on the same substrate the threshold voltages may be different by up to 1.75 V (e.g. table in col. 3).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the threshold voltages of the two power transistors of a monolithic structure differ by over 0.1 V, since Green teaches that such modifications are known in the art. One would be motivated to make such a modification in order to allow for more flexibility in circuit design, as well as for an increase in transistor switching speed, as disclosed in Green (col. 3, lines 52 - 53, and col. 4, lines 33 - 34).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 4146
February 15, 2008

/Marvin M. Lateef/
Supervisory Patent Examiner, Art Unit 4146